What is claimed is:

1. A timing loop controller for multilevel modulation scheme, comprising:

a first buffer for orderly receiving I-channel digital signals and generating first buffered signals by buffering the received I-channel digital signals;

a second buffer for receiving the received I-channel digital signals from the first buffer and generating second buffered digital signals;

a first quantization means for receiving the buffered digital signals from the second buffer and generating first quantized signals by quantizing the second buffered digital signals;

a second quantization means for receiving the I-channel digital signals and generating second quantized signals by quantizing the I-channel digital signals;

a first sign detection means for receiving the first quantized signals and the second quantized signals and detecting sign change of the first quantized signals and the second quantized signals;

a third buffer for orderly receiving Q-channel digital signals and generating a third buffered signals by buffering the received Q-channel digital signals;

a fourth buffer for receiving the received Q-channel digital signals from the first buffer and generating fourth buffered digital signals;

a third quantization means for receiving the fourth buffered digital signals from the fourth buffer and generating third quantized signals by quantizing the fourth buffered digital signals;

a fourth quantization means for receiving the Q-channel digital signals and generating fourth quantized signals by quantizing the Q-channel digital signals;

a second sign detection means for receiving the third quantized signals and the fourth quantized signals and detecting sign change of the third quantized signals and the fourth quantized signals;

a timing error computation means for computing a timing error output value based on the I-channel digital signals, the first buffered signals, the first quantized signals, the Q-channel digital signals, the third buffered signals, the third quantized signals and the fourth quantized signals;

a zero crossing detection means for detecting zero crossing at I axis and Q axis according based on results outputted from the first and second sign detection means; and

a timing error control means for controlling the timing error value in case there is no sign change according to results outputted from the first and second sign detection means.

2. The timing loop controller as recited in claim 1,

wherein the timing error computation means computes an error value (ε_n) by following equation as:

$$\varepsilon_n = \overline{I_{2n-1}}(\overline{I_{2n}} - \overline{I_{2n-2}}) + \overline{Q_{2n-1}}(\overline{Q_{2n}} - \overline{Q_{2n-2}})$$

$$\overline{I_{2n-1}} = (I_{2n-1} - 0.5 \bullet (I_{2n} + I_{2n-2}))$$
$$\overline{Q_{2n-1}} = (Q_{2n-1} - 0.5 \bullet (Q_{2n} + Q_{2n-2}))$$
$$\overline{I_{2n}} = 0.5 \bullet I_{2n},\ \overline{Q_{2n}} = 0.5 \bullet Q_{2n}$$
$$\overline{I_{2n-2}} = 0.5 \bullet I_{2n-2},\ \overline{Q_{2n-2}} = 0.5 \bullet Q_{2n-2}$$

wherein the n is nature number bigger than 1, $\overline{I_{2n}}$ is the I-channel digital signal, $\overline{I_{2n-1}}$ is the first buffered signal, $\overline{I_{2n-2}}$ is the first quantized signal, $\overline{Q_{2n}}$ is the Q-channel digital signal, $\overline{Q_{2n-1}}$ is the third buffered signal, $\overline{Q_{2n-2}}$ is the third quantized signal.

3. A symbol timing synchronizer using a timing synchronous loop controller for multilevel modulation scheme, comprising:

A/D conversion means for converting successively inputted analogue signals to digital signals;

timing error detection means for calculating an timing error between an input timing of the digital signal successively inputted from the A/D conversion means and a sampling timing of the A/D conversion means and detecting sign change of the digital signals;

timing error output control means for outputting the timing error calculated from the timing error detection means and controlling the timing error output value;

filtering means for eliminating a noise of the timing error value controlled by the timing error output control means and calculating a mean value of errors; and

timing error compensation means for compensating the timing error of the sampling timing of the A/D conversion means by shifting the sampling timing corresponding to the calculated error value from the timing error detection means.

4. The symbol timing synchronizer as recited in claim 3, wherein the timing error detection means includes:

a first buffer for orderly receiving I-channel digital signals and generating first buffered signals by buffering the received I-channel digital signals;

a second buffer for receiving the received I-channel digital signals from the first buffer and generating second buffered digital signals;

a first quantization means for receiving the buffered digital signals from the second buffer and generating first quantized signals by quantizing the second buffered digital signals;

a second quantization means for receiving the I-channel digital signals and generating second quantized signals by quantizing the I-channel digital signals;

a first sign detection means for receiving the first quantized signals and the second quantized signals and detecting sign change of the first quantized signals and

the second quantized signals;

a third buffer for orderly receiving Q-channel digital signals and generating a third buffered signals by buffering the received Q-channel digital signals;

a fourth buffer for receiving the received Q-channel digital signals from the first buffer and generating fourth buffered digital signals;

a third quantization means for receiving the fourth buffered digital signals from the fourth buffer and generating third quantized signals by quantizing the fourth buffered digital signals;

a fourth quantization means for receiving the Q-channel digital signals and generating fourth quantized signals by quantizing the Q-channel digital signals;

a second sign detection means for receiving the third quantized signals and the fourth quantized signals and detecting sign change of the third quantized signals and the fourth quantized signals;

a timing error computation means for computing a timing error output value based on the I-channel digital signals, the first buffered signals, the first quantized signals, the Q-channel digital signals, the third buffered signals, the third quantized signals and the fourth quantized signals;

a zero crossing detection means for detecting zero crossing at I axis and Q axis according based on results outputted from the first and second sign detection means;

and

a timing error control means for controlling the timing error value in case there is no sign change according to results outputted from the first and second sign detection means.

5. The symbol timing synchronizer as recited in claim 3, wherein the timing error computation means computes an error value (ε_n) by following equation as:

$$\varepsilon_n = \overline{I_{2n-1}}(\overline{I_{2n}} - \overline{I_{2n-2}}) + \overline{Q_{2n-1}}(\overline{Q_{2n}} - \overline{Q_{2n-2}})$$

$$\overline{I_{2n-1}} = (I_{2n-1} - 0.5 \bullet (I_{2n} + I_{2n-2}))$$
$$\overline{Q_{2n-1}} = (Q_{2n-1} - 0.5 \bullet (Q_{2n} + Q_{2n-2}))$$
$$\overline{I_{2n}} = 0.5 \bullet I_{2n},\ \overline{Q_{2n}} = 0.5 \bullet Q_{2n}$$
$$\overline{I_{2n-2}} = 0.5 \bullet I_{2n-2},\ \overline{Q_{2n-2}} = 0.5 \bullet Q_{2n-2}$$

wherein the n is nature number bigger than 1, $\overline{I_{2n}}$ is the I-channel digital signal, $\overline{I_{2n-1}}$ is the first buffered signal, $\overline{I_{2n-2}}$ is the first quantized signal, $\overline{Q_{2n}}$ is the Q-channel digital signal, $\overline{Q_{2n-1}}$ is the third buffered signal, $\overline{Q_{2n-2}}$ is the third quantized signal.

6. The symbol timing synchronizer as recited in claim 3, wherein the timing error detection means outputs the timing error by using the zero crossing detection means and detects and traces the timing error by controlling the timing error output signal by equipping a gain controlled loop at back of an output terminal of the timing error

detection means in case of a modulation method having less zero crossing.

7. The symbol timing synchronizer as recited in claim 3, wherein the timing error output control means controls the timing error output value in only case that there is no sign change according to a detection result of the first and second sign detectors.

8. A method implemented for synchronizing symbol timing by using a timing synchronous loop controller, the method comprising the steps of:

a) converting successively inputted analogue signals to digital signals by an A/D conversion unit;

b) calculating an timing error between an input timing of the digital signal successively inputted from the A/D conversion unit and a sampling timing of the A/D conversion unit and detecting sign change of the digital signals by a timing error detection unit;

c) outputting the timing error calculated from the timing error detection unit and controlling the timing error output value;

d) eliminating a noise of the timing error value and calculating a mean value of errors; and

e) compensating the timing error of the sampling timing of the A/D conversion unit by shifting the sampling timing corresponding to the calculated error value from the

timing error detection unit.

9. The method as recited in claim 8, wherein the step b) includes the steps of:

b1) computing a timing error between an input timing of orderly inputted digital signals and a sampling timing;

b2) controlling a direction and an error value of the timing error;

b3) detecting sign change according to results of step b2);

b4) detecting zero crossing at I axis and Q axis according to results outputted from the step b3); and

b5) controlling the timing error value in case there is no sign change according to results of step b4).

10. The method as recited in claim 9, wherein the step c) controls the timing error output value according to the result of the sign variation detector in case there is no sign variation.

11. A computer readable recoding medium for storing instructions for executing a method for synchronizing symbol timing by using a timing synchronous loop controller, the method comprising the steps of:

a) converting successively inputted analogue signals to digital signals by an A/D conversion unit;

b) calculating an timing error between an input

timing of the digital signal successively inputted from the A/D conversion unit and a sampling timing of the A/D conversion unit and detecting sign change of the digital signals by a timing error detection unit;

c) outputting the timing error calculated from the timing error detection unit and controlling the timing error output value;

d) eliminating a noise of the timing error value and calculating a mean value of errors; and

e) compensating the timing error of the sampling timing of the A/D conversion unit by shifting the sampling timing corresponding to the calculated error value from the timing error detection unit.